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Nicole Barrese  
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	
In re application of: <b>Huilong Zhu, et al.</b>	Date: <b>December 13, 2004</b>
Serial Number: <b>10/709,239</b>	Examiner:
Filed: <b>4/23/2004</b>	Group Art Unit: <b>2811</b>
Title: <b>STRUCTURES AND METHODS FOR MANUFACTURING OF DISLOCATION FREE STRESSED CHANNELS IN BULK SILICON AND SOI CMOS DEVICES BY GATE STRESS ENGINEERING WITH SiGe AND/OR Si:C</b>	IBM Corporation D/18G, B/300, Zip 482 2070 Route 52 Hopewell Junction, NY 12533-6531

### INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to the duty of disclosure set forth in 37 C.F.R. 1.56, and further pursuant to the provisions of 37 C.F.R. 1.97 and 1.98, applicants hereby respectfully submit copies of the non-US patents and publications as listed on Form PTO-1449, attached hereto.

In citing these documents, no representation is made nor intended as to the pertinency or non-pertinency of the art, that better art than that listed is not available, or that other art is not applicable.

No fee is believed to be due for this submission. If any fees are required, however, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,  
Huilong Zhu, et al.

By:

Joseph P. Abate 12-13-04  
Joseph P. Abate  
Registration No. 30,238  
Telephone: (845) 894-4633

FIS920030375

FORM PTO-1449 (Modified)		ATTY. DOCKET NO. FIS920030375	SERIAL NO. 10/709,239
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT		APPLICANT: Huilong Zhu, et al.	
(Use several sheets if necessary)		FILING DATE: 4/23/04	GROUP: 2811

## REFERENCE DESIGNATION

## U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	6,228,694 B1	5/8/2001	Doyle et al.			
	6,406,973 B1	6/18/2002	Lee			
	6,281,532 B1	8/28/2001	Doyle et al.			
	5,683,934	11/4/97	Candelaria			
	6,368,931 B1	4/9/2002	Kuhn, et al.			
	5,310,446	5/10/94	Konishi et al.			
	4,853,076	8/1/89	Tsaur et al.			
	US 2002/0090791 A1	7/11/2002	Doyle et al.			
	US 2002/0074598 A1	6/20/2002	Doyle et al.			
	6,509,618 B2	1/21/2003	Jan et al.			
	6,476,462 B2	11/5/2002	Shimizu et al.			
	6,362,082 B1	3/26/2002	Doyle et al.			
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	5,565,697	10/15/96	Asakawa et al.			
	US 2003/0040158 A1	2/27/2003	Saitoh			
	US 2002/0086472 A1	7/4/2002	Roberds et al.			
	6,521,964 B1	2/18/2003	Jan et al.			
	6,506,652	01/14/03	Jan, et al.			

## FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
					YES	NO

## OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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REFERENCE DESIGNATION			U.S. PATENT DOCUMENTS				
EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
		5,081,513	1/14/1992	Jackson, et al.			
		3,602,841	8/31/1971	McGroddy			
		6,531,740	3/11/2003	Bosco, et al.			
		6,531,369	3/11/2003	Ozkan, et al.			
		6,501,121	12/31/2002	Yu, et al.			
		6,498,358	12/24/2002	Lach, et al.			
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		6,403,975	6/11/2002	Brunner, et al.			
		6,361,885	3/26/2002	Chou			
		6,255,169	7/3/2001	Li, et al.			
		6,246,095	6/12/2001	Brady, et al.			
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		6,133,071	10/17/2000	Nagai			
		6,046,464	4/4/2000	Schetzina			
		6,025,280	2/15/2000	Brady, et al.			

  

FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO
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REFERENCE DESIGNATION		U.S. PATENT DOCUMENTS					
EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
		5,940,736	8/17/1999	Brady, et al.			
		5,880,040	3/9/1999	Sun, et al.			
		5,861,651	1/19/1999	Brasen, et al.			
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		5,391,510	2/21/1995	Hsu, et al.			
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		5,108,843	4/28/1992	Ohtaka, et al.			
		5,060,030	10/22/1991	Hoke			
		4,958,213	9/18/1990	Eklund, et al.			
		4,665,415	5/12/1987	Esaki, et al.			
		6,635,506	10/21/2003	Volant et al.			

  

FOREIGN PATENT DOCUMENTS							
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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	5,989,978	11/23/1999	Peidous			
	6,284,626	9/4/2001	Kim			
	6,274,444	8/14/2001	Wang			
	6,261,964	7/17/2001	Wu, et al.			
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	6,117,722	9/12/2000	Wuu, et al.			
	6,107,143	8/22/2000	Park, et al.			
	6,090,684	7/18/2000	Ishitsuka, et al.			
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	5,557,122	9/17/1996	Shrivastava, et al.			
	5,354,695	10/11/1994	Leedy			
	5,134,085	7/28/1992	Gilgen, et al.			
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	6,621,392	09-16-2003	Volant et al.			

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FORM PTO-1449 (Modified)

LIST OF PATENTS AND PUBLICATIONS  
FOR APPLICANT'S INFORMATION  
DISCLOSURE STATEMENT

Docket Number (Optional)

FIS920030375

Application Number

10/709,239

Applicant(s)

Huiliong Zhu, et al.

Filing Date

4/23/04

Group Art Unit

2811

## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		5,940,716	8/17/1999	Jin, et al.			

## FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

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Supplemental FORM PTO-1449 (Modified)	ATTY. DOCKET NO. FIS920030375	SERIAL NO. 10/709,239
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FOREIGN PATENT DOCUMENTS
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DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
					YES NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)
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	Kern Rim, et al., "Transconductance Enhancement in Deep Submicron Strained-Si <i>n</i> -MOSFETs", International Electron Devices Meeting, 26, 8, 1, IEEE, September 1998.
	Kern Rim, et al., "Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs", 2002 Symposium On VLSI Technology Digest of Technical Papers, IEEE, pp 98-99.
	Gregory Scott, et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress", International Electron Devices Meeting, 34.4.1, IEEE, September 1999.
	F. Ootsuka, et al., "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Application", International Electron Devices Meeting, 23.5.1, IEEE, April 2000.
	Shinya Ito, et al., "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design", International Electron Devices Meeting, 10.7.1, IEEE, April 2000.
	A. Shimizu, et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement", International Electron Devices Meeting, IEEE, March 2001.
	K. Ota, et al., "Novel Locally Strained Channel Technique for high Performance 55nm CMOS", International Electron Devices Meeting, 2.2.1, IEEE, February 2002.

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